WHAT IS CLAIMED IS:

1. A field effect transistor comprising:

a channel having a first doped region and a second doped region underlying the first doped region;

a source adjacent to the channel; and

a drain adjacent to the channel.

2. The field effect transistor of Claim 1, wherein the first doped region comprises a first concentration of a dopant, and wherein the second doped region comprises a second concentration of the dopant, the first concentration being greater than the second concentration.

3. The field effect transistor of Claim 2, wherein the dopant comprises an n-type dopant.

4. The field effect transistor of Claim 1, wherein the first doped region comprises a first dopant, and wherein the second doped region comprises a second dopant different from the first dopant.

5. The field effect transistor of Claim 4, wherein the first dopant comprises arsenic, and wherein the second dopant comprises phosphorus.

6. The field effect transistor of Claim 1, further comprising a first pocket surrounding the source and a second pocket surrounding the drain, the first and second pockets each having a higher dopant concentration than the source and drain regions.

Sub B2

7. A semiconductor device comprising a plurality of field effect transistors, at least one of the field effect transistors having a channel comprising a subsurface doped layer, the field effect transistor further having a source adjacent to the channel, a drain adjacent to the channel and a gate overlying the channel.

8. The semiconductor device of Claim 7, wherein the channel of the field effect transistor further comprises a surface doped layer overlying the subsurface doped layer.

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9. The semiconductor device of Claim 8, wherein the surface doped layer comprises a first concentration of a dopant, and wherein the subsurface doped layer comprises a second concentration of the dopant, the first concentration being greater than the second concentration.

10. The semiconductor device of Claim 9, wherein the dopant comprises an n-type dopant.

11. The semiconductor device of Claim 8, wherein the surface doped layer comprises a first dopant, and wherein the subsurface doped layer comprises a second dopant different from the first dopant.

12. The semiconductor device of Claim 11, wherein the first dopant comprises arsenic, and wherein the second dopant comprises phosphorus.

13. The semiconductor device of Claim 7, further comprising a first doped pocket surrounding the source and a second doped pocket surrounding the drain, the first and second pockets each having a higher dopant concentration than the source and drain regions.

Sub B3

14. A method for forming a field effect transistor, comprising the steps of:

implanting a first dopant in a subsurface channel region;

forming a gate over the subsurface channel region; and

implanting a second dopant in a source/drain region adjacent to the subsurface channel region.

15. The method of Claim 14, further comprising the step of implanting a third dopant in a surface channel region overlying the subsurface channel region.

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16. The method of Claim 14, further comprising the step of implanting a fourth dopant in a pocket surrounding the source/drain region.

17. The method of Claim 15, wherein the first dopant comprises phosphorus, and wherein the second dopant comprises a p-type dopant, and wherein the third dopant comprises arsenic.